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UNITED STATES PATENT APPLICATION

FOR

A SYSTEM FOR CLOCK DUTY CYCLE STABILIZATION

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A SYSTEM FOR CLOCK DUTY CYCLE STABILIZATION

TECHNICAL FIELD

The present invention relates to the field of mixed signal
10 integrated circuit devices. More particularly, the present invention
relates to the provision of high-quality clock signals for analog-to-digital
converter integrated circuit devices.

BACKGROUND ART

15 Modern Analog to Digital Converters (ADCs) are timed based on a
user supplied low jitter external clock source. These ADCs often operate
on both phases of this clock signal to increase both efficiency and
throughput. ADCs are specified to operate with a clock signal having a
duty cycle that varies across a certain range. As is well known, a clock
20 signal's duty cycle refers to a ratio of one clock phase width to the entire
clock period. An ADC capable of operating over a wider duty cycle
range can be beneficial in that the ADC is more flexible and useful
across a larger set of applications.

25 A problem exists with prior art ADCs having the capability of
operating over a wider clock signal duty cycle. Such prior art ADCs
have internal circuitry configured to function with wide-ranging duty
cycles. This circuitry unfortunately also increases the power needed to

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achieve high performance. Excessive power requirements leads to a number of disadvantages. For example, in handheld applications, an excessive power requirement reduces the battery life of a device. In other applications, excessive power requirements can lead to heat
5 dissipation problems, noise problems, and other types of unreliability effects.

Thus, what is required is a solution for implementing duty cycle stabilization for an ADC integrated circuit device. The required
10 solution should be capable of producing a clock signal having a duty cycle that is independent of any external clock duty cycle. Additionally, the required solution should be capable of producing a clock signal having a near optimal duty cycle of 50% for lowest power consumption in most ADCs. The present invention provides a novel
15 solution to these requirements.

SUMMARY OF THE INVENTION

Embodiments of the present invention provide a solution for implementing duty cycle stabilization for an ADC integrated circuit device. Embodiments of the present invention are capable of producing
5 a clock signal having a duty cycle that is independent of any external clock duty cycle. Additionally, embodiments of the present invention are capable of producing a clock signal having a near optimal duty cycle of 50% for lowest power consumption in most ADCs.

10 In one embodiment, the present invention is implemented as a clock signal duty cycle stabilization circuit for producing a high-quality internal clock signal. The circuit includes an edge detection circuit and a latch circuit. The edge detection circuit is configured to receive an external clock signal (e.g., a reference clock signal produced by an
15 external VCO, a crystal oscillator, a high quality sine source, etc.) and generate an output therefrom. The latch circuit is coupled to receive the output from the edge detection circuit. The latch circuit is configured to produce a rising edge of the internal clock signal and a falling edge of the internal clock signal in accordance with the output of
20 the edge detection circuit. The duty cycle of the internal clock signal is very stable and is substantially independent of duty cycle variations of the external clock signal.

In one embodiment, the edge detection circuit comprises a NAND
25 gate coupled to a delay element, wherein the NAND gate has an input to receive the external clock signal and an output for producing the output of the edge detection circuit. In one embodiment, the latch circuit comprises an R-S latch, wherein the R-S latch is configured to receive the output of the edge detection circuit and generate the rising

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edge and the falling edge therefrom. Additionally, in one embodiment, the internal clock signal is a 50% duty cycle clock signal for use by an ADC.

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BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not by way of limitation, in the Figures of the accompanying drawings and in which like reference numerals refer to similar elements and in
5 which:

Figure 1 shows a diagram of a PLL circuit in accordance with one embodiment of the present invention.

10 Figure 2 shows a diagram depicting the outputs of the VCRO in accordance with one embodiment of the present invention.

Figure 3 shows a diagram depicting the internal components of a clock duty cycle stabilization circuit used to generate a high quality
15 internal clock signal in accordance with one embodiment of the present invention.

Figure 4 shows a timing diagram depicting the signals from the stabilization circuit of Figure 3 as shown.

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Figure 5 shows a diagram depicting the internal components of a clock duty cycle stabilization circuit used to generate a high quality internal clock signal in accordance with an alternative embodiment of the present invention.

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Figure 6 shows the signal timing diagram for the stabilization circuit of Figure 5.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be understood by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Figure 1 shows a diagram of a PLL (phase locked loop) circuit 100 in accordance with one embodiment of the present invention. As depicted in Figure 1, the PLL 100 includes a voltage controlled ring oscillator 120 coupled to receive a VCO control voltage 115 produced by a phase comparison unit 105 and phase difference unit 110.

The PLL 100 of the present embodiment is an exemplary PLL suitable for use with modern integrated circuit devices, such as, for example, highly integrated SOC (system-on-a-chip) devices. New SOCs are emerging with ADCs along with PLLs used for data formatting. The PLLs are usually comprised of a control loop (e.g., feedback clock 125)

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and a Voltage Controlled Oscillator (VCO). Internal VCOs are often realized as Voltage Controlled Ring Oscillators (VCROs), shown in PLL 100 as VCRO 120. VCRO 120 comprises rings of inverting stages that naturally oscillate and whose frequency can be changed by a control
5 voltage, the VCO control voltage 115. The outputs 130 of the VCRO 120 are as shown.

The action of the PLL 100 can be used to lock the VCRO 120 frequency to an external clock (e.g., reference clock 101) frequency.
10 VCROs often produce a nearly 50% Duty Cycle oscillation because the oscillation waveform must propagate twice through the Ring Oscillator before it returns to its initial state. The two propagations usually have same delay.

15 Figure 2 shows a diagram depicting the outputs 130 of the VCRO 120 in accordance with one embodiment of the present invention. As shown in Figure 2, PLL 100 is a conventional PLL having typical phase noise/jitter performance. In the prior art, high performance VCROs incurred penalties with respect to increased power consumption.
20 Additionally, in the prior art, PLLs configured for low power consumption usually produce higher jitter and therefore cannot be used as high performance ADC clocks. In contrast, the clock stabilization embodiments of the present invention enable the production of a high quality, low phase noise/jitter, 50% duty cycle internal clock signals,
25 while using a conventional PLL, such as PLL 100, having typical phase noise/jitter.

Figure 3 shows a diagram depicting the internal components of a clock duty cycle stabilization circuit 300 used to generate a high

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quality internal clock signal in accordance with one embodiment of the present invention. As shown in Figure 3, the clock duty cycle stabilization circuit 300 (e.g., or simply the stabilization circuit 300) includes an edge detection circuit having a first and second portion
5 310-311, coupled to a latch circuit 320.

In the present embodiment, the stabilization circuit 300 functions in part by producing a high-quality internal clock signal, the ADC clock 340. The edge detection circuit 310-311 is configured to
10 receive an external clock signal (e.g., a reference clock signal 335 produced by an external VCO) and generate an output therefrom. In the present embodiment, the output of the edge detection circuit 310-311 is the outputs 345-350 (e.g., Trigger A and Trigger B) as shown. The outputs 345-350 are coupled to the latch circuit 320. The latch
15 circuit 320 is coupled to receive the outputs 345-350 and to produce a rising edge of the internal clock signal 340 and a falling edge of the internal clock signal 340 in accordance therewith. The duty cycle of the internal clock signal 340 is very stable and is substantially independent of duty cycle variations of the external reference clock
20 signal 335.

In one embodiment, the edge detection circuit comprises a NAND gate coupled to a delay element, wherein the NAND gate has an input to receive the external clock signal and an output for producing the
25 output of the edge detection circuit. In one embodiment, the latch circuit 320 comprises an R-S latch, wherein the R-S latch is configured to receive the output of the edge detection circuit and generate the rising edge and the falling edge therefrom. Additionally, in one

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embodiment, the internal clock signal 340 is a 50% duty cycle clock signal for use by an ADC 360.

In the present embodiment, each of the portions 310-311 of the edge detection circuit comprises a respective NAND gate coupled to a delay element. The NAND gate 318 of the portion 311 has an input to receive the external clock signal 335 and an output for producing the output 350 of the edge detection circuit. The NAND gate 315 of the portion 310 has an input to receive a conditioned signal 330 (e.g., VCRO edge Ab) and an output for producing the output 345 of the edge detection circuit.

The conditioned signal 330 is produced in accordance with the reference clock signal 335. The conditioned signal is a one half period delayed signal (with respect to the external clock signal 335) used to produce the falling edge of the internal clock signal 340. The conditioned signal is produced by the conditioning circuit. It should be noted that there are a number of different types of circuits that can be used to produce the conditioned signal, such as, for example, an RC delay circuit, an inverter delay circuit, and the like.

The conditioned signal 330 is used by the edge detection circuit portion 310 as shown. The external reference clock signal 335 is a reference clock signal from an external source, such as, for example, an external VCO, a crystal oscillator, a high quality sine source, or the like. The conditioned signal 330 passes through an inverter 313 and a delay element 314 and to the NAND gate 315. The external reference clock signal 335 passes through an inverter 316 and a delay element 317 and to the NAND gate 318.

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In the present embodiment, the latch circuit 320 comprises an R-S latch. The R-S latch 320 is configured to receive the output 345-350 of the edge detection circuit and generate the rising edge and the falling edge of the internal clock signal 340 therefrom. In the present
5 embodiment, this internal clock signal 340 is a highly stable 50% duty cycle clock signal for use by an analog to digital converter 360.

Figure 4 shows a timing diagram depicting the signals 330, 345,
10 335, 350, and 340 from the stabilization circuit 300 of Figure 3 as shown. As depicted in Figures 3 and 4, the stabilization circuit 300 employs the edge detection circuitry 310-311 and the latch 320 to form the internal clock signal 340. During the operation of the edge detection circuit 310-311, a signal is applied to the input of the NAND
15 and through the delay to the input of the NAND. The resulting output (e.g., signals 345 and 350) is a negative glitch following a rising edge of the input signal. This glitch is used to Set or Reset the state of the latch 320 (e.g., an R-S latch). The rising edge of the external reference clock signal 335 causes the R-S latch 320 to transition from Reset to Set or
20 "0" to "1", thereby creating a rising output. The edge of the conditioned signal 330 (e.g., VCRO edge Ab) causes the R-S latch 320 to transition from Set to Reset or "1" to "0", thereby creating a falling output. The R-S latch 320 output is fed to clock timing circuits making sure the output rising edge is associated with the ADC 360 input
25 sampling edge.

Thus, a low jitter 50% duty cycle clock 340 can be produced by using information from both the external low jitter clock 335 and the internal higher jitter VCRO 330. Sampling noise is introduced to an

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ADC 360 by the jitter on the clock edge associated with sampling the input signal. In ADC systems which sample the input signal only once per clock cycle, only the sampling edge of the clock must exhibit low jitter behavior. The opposite edge is non critical and can contain more
5 jitter. The internal 50% duty cycle clock can be produced then by using the external clock 335 to generate the sampling edge and the internal VCRO 330 to generate the non-critical edge.

It should be noted that PLLs often lock their reference input clock
10 edge to one VCRO stage output edge "edgeA". Seeing as these two edges are aligned, the inverse edge of stage A "edgeAb" 330 occurs exactly one half clock cycle after the reference edge 335. In the present embodiment, the internal clock 340 is generated by triggering a sample edge transition off the reference clock edge 335 and a non
15 critical edge off edgeAb 330.

Figure 5 shows a diagram depicting the internal components of a clock duty cycle stabilization circuit 500 used to generate a high quality internal clock signal in accordance with an alternative
20 embodiment of the present invention. The circuit 300 embodiment generates a stand alone internal 50% duty cycle clock 340 which is then distributed to the ADC 360 clock timing generator. The circuit 500 embodiment distributes the reference clock edge and "edgeAb" to each timing generator and the 50% duty cycle is formed there.

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The circuit 500 embodiment is much like the circuit 300 embodiment, yet it differs in the ADC timing. The associated signal timing diagram of stabilization circuit 500 is shown in Figure 6. Switched-Capacitor ADCs usually have a non-overlapping clock timing

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generators which can be constructed as R-S latches with longer feedback delays. In the circuit 500 embodiment, the reference clock rising edge detection circuit portion 311 is used to set a non-overlapping clock generator 501. This setting is associated with the sampling edge
5 of the ADC 360. The VCRO edge detection circuit portion 310 is used to reset the non-overlapping clock generator 501. This resetting is associated with the non-critical timing edges. For proper operation, the delay in the edge detection circuitry 310-311 needs to be greater than or equal in delay to a feedback path of the non-overlapping clock
10 generator 501. The clock generator 501 produces the sample signals 505 and 506, and the hold signals 507 and 508 as shown.

Figure 6 shows the signal timing diagram for the stabilization circuit 500 of Figure 5. As depicted in Figure 6, the timing of the
15 signals 330, 345, 507, 508, 335, 350, 505, and 506 are shown. The trigger width arrow 601 points out the delay required for proper operation, where the delay in the edge detection circuitry 310-311 needs to be greater than or equal in delay to a feedback path of the non-overlapping clock generator 501. Thus, by using either the circuit 300
20 embodiment or the circuit 500 embodiment, a high performance 50% duty cycle clock can be created internally regardless of the external clock duty cycle. The 50% duty cycle leads to reduced design constraints and lower power operation for the ADC.

25 The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications and variations are possible in light of the above teaching. The embodiments

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were chosen and described in order best to explain the principles of the invention and its practical application, thereby to enable others skilled in the art best to utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated.

- 5 It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

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